Amendments to the Claims are reflected in the listing of claims that begins on page 3 of this paper.

Remarks/Arguments begin on page 10 of this paper.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (original) A system interface comprising:

(a) a plurality of first director boards, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and a pair of output/input ports;

(b) a plurality of second director boards, each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and a pair of output/input ports;

(c) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) a message network, operative independently of the data transfer section, such message network comprising:

a pair of message network boards, each one of such message network boards having:

a switching network having a plurality input/output ports, each one of such pair of input/output ports being coupled to a corresponding one of the pair of output/input ports of the crossbar switches of the plurality of first director boards and the plurality of second director boards; and

(e) wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors

and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

2. (original) The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

3. (original) The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

4. (original) The system interface recited in claim 2 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

5. (original) The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

6. (original) The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

7. (original) The system interface recited in claim 5 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

8. (original) A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

(a) a plurality of first director boards coupled to host computer/server; each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and a pair of output/input ports;

(b) a plurality of second director boards coupled to the bank of disk drives, each one of the second director boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and a pair of output/input ports;

(c) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) a message network, operative independently of the data transfer section, such message network comprising:

a pair of message network boards, each one of such message network boards having:

a switching network having a plurality input/output ports, each one of such pair of input/output ports being coupled to a corresponding one of the pair of output/input ports of the crossbar switches of the plurality of first director boards and the plurality of second director boards; and

(e) wherein the first and second directors control data transfer between the host computer and the bank of disk drives in response to messages passing between the first directors and the second directors through the message network to facilitate the data transfer between host computer/server and the bank of disk drives with such data passing through the cache memory in the data transfer section.

9. (original) The system interface recited in claim 8 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

10. (original) The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

11. (original) The system interface recited in claim 9 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

12. (original) The system interface recited in claim 8 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and

for controlling the data between the input of such one of the first directors and the cache memory.

13. (original) The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

14. (original) The system interface recited in claim 12 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

15. (new) The system interface recited in claim 1 wherein the messaging network is configured to couple any one of the first directors to a selected one of said second directors and to couple to any one of the second directors to a selected one of said first directors.

16. (new) The system recited in claim 8 wherein the messaging network is configured to couple any one of the first directors to a selected one of said second directors and to couple to any one of the second directors to a selected one of said first directors.